WHAT IS CLAIMED IS :

1. A method for fabricating a semiconductor device comprising:

forming a device isolation region on a semiconductor substrate to define a cell array region and a peripheral circuit region;

forming a first gate in the cell array region, a second gate in the peripheral circuit region, and a third gate in the peripheral circuit region;

implanting first impurity ions of a low concentration into a first portion of the semiconductor substrate adjacent to the second and third gates, using the second and third gates as a mask, to form a first impurity diffusion region of a first conductivity type;

forming first gate spacers on lateral sides of the first, second, and third gates;

implanting second impurity ions of a low concentration into a second portion of the semiconductor substrate adjacent to the first gate and first gate spacers, using the first gate and first gate spacers as a mask, to form a second impurity diffusion region of a first conductivity type;

implanting third impurity ions of a low concentration into a third portion of the semiconductor substrate adjacent to the third gate and first gate spacers, using the third gate and first gate spacers as a mask, to form a third impurity diffusion region of a second conductivity type;

forming an insulating layer over the semiconductor substrate, first through third gates, and first gate spacers;

etching the insulating layer in the peripheral region to form second gate spacers adjacent to the first spacers adjacent to the second and third gates;

implanting fourth impurity ions of a high concentration into a fourth portion of the semiconductor substrate adjacent to the second gate and second spacers, using the second gate and first and second spacers as a mask, to form a fourth impurity diffusion region of a first conductivity type; and

implanting fifth impurity ions of a high concentration into a fifth portion of the semiconductor substrate adjacent to the third gate and second spacers, using the third gate and first and second spacers as a mask, to form a fifth impurity diffusion region of a second conductivity type.

2. A method for fabricating a semiconductor device, as recited in claim 1, wherein the first conductivity type is n-type.

3. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of first impurity ions has a lower ion diffusivity than the step of implanting second impurity ions.

4. A method for fabricating a semiconductor device, as recited in claim 1, wherein the first through third gates comprise polysilicon.

5. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of first impurity ions is performed using arsenic with a dose range of about $5x10^{12}$ ions/cm^2 and at an energy range of about 50 keV.

6. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of second impurity ions is performed using phosphorous with a dose range of about $5x10^{12}$ ions/cm^2 and at an energy range of about 30 keV.

7. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of third impurity ions is performed using boron or BF_3 with a dose range of about $1x10^{13}$ ions/cm^2 and at an energy range of about 20 keV.

8. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of fourth impurity ions is performed using arsenic with a dose range of about $5x10^{15}$ ions/cm^2 and at an energy range of about 50 keV.

9. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of fifth impurity ions is performed using boron or BF_3 with a dose range of about $5x10^{15}$ ions/cm^2 and at an energy range of about 20 keV.

10. A method for fabricating a semiconductor device, as recited in claim 1, further comprising:

forming a silicide layer over the semiconductor substrate, the second gate, and the third gate in the peripheral circuit region; and

forming an interlayer insulating layer over the substrate and first through third gates;

etching a selected portion of the interlayer insulating layer in the cell array region, using the insulating layer as for an etching stopper, and forming a contact opening adjacent to the first gate.

11. A method for fabricating a semiconductor device, as recited in claim 10, wherein the forming of a silicide layer is further comprises

forming a transition metal over the substrate and the second and third gates

annealing the substrate and the transition metal to form the silicide layer.

12. A method for fabricating a semiconductor device, as recited in claim 11, wherein during the annealing of the substrate and the transition ,metal, the first through fifth impurities are diffused into the first through fifth impurity diffusion regions, respectively.

13. A method for fabricating a semiconductor device, as recited in claim 10, wherein the a remaining portion of the insulating layer, after the etching of the insulating layer in the peripheral region, serves as a barrier layer to prevent silicidation in the cell array area during the forming of a silicide layer.

14. A method for fabricating a semiconductor device, as recited in claim 10, wherein the interlayer insulating layer has a first etching rate at least five times as high as a second etching rate of the insulating layer.

15. A method for fabricating a MOS transistor in a semiconductor device, the method comprising the steps of:

forming a gate electrode over a semiconductor substrate;

implanting first impurity ions at a low concentration of a first conductivity type, using the gate electrode as a mask, to form a first impurity diffusion layer;

forming first spacers on lateral sides of the gate;

implanting second impurity ions at a low concentration of a second conductivity type, using the gate and first spacers as a mask, to form a second impurity diffusion layer;

forming a second spacers adjacent to the first spacers;

implanting third impurity ions of high concentration of a second conductivity type, using the gate and the first and second spacers as a mask, to form a third impurity diffusion layer; and

annealing and diffusing the impurity diffusion layers to overlap the first diffusion layer with the second diffusion layer.

16. A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the first conductivity type is n-type.

17. A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the implanting of first impurity ions is performed using arsenic with a dose range of about $5x10^{12}$ ions/cm^2 and at an energy range of about 50 keV.

18. A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the implanting of second impurity ions is performed using boron or BF_3 with a dose range of about $1x10^{13}$ ions/cm^2 and at an energy range of about 20 keV.

19. A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the implanting of third impurity ions is performed using boron or BF_3 with a dose range of about $5x10^{15}$ ions/cm^2 and at an energy range of about 20 keV.